

#### Introduction

#### Background

- Hydrodynamics codes require material specific thermodynamic data, usually obtained with an analytic or tabular equation of state (EOS)
- EOSPAC is a library that provides access to and interpolation routines for material data tables
- FleCSALE is a continuum dynamics code that is built on the FleCSI framework and uses EOSPAC
- FleCSI is a compile-time configurable framework designed to support multi-physics application development

#### **Objective**

- Optimize FleCSALE in the context of EOSPAC by investigating: EOSPAC library optimizations, hybrid programming for FleCSALE, and FleCSI sparse data optimizations
- All scaling simulations were run on Broadwell CPUs to a simulation time of 1.5s



Figure 1: Initial communication and computation breakdown of FleCSALE

### **Strategies for EOSPAC**

#### **Optimizing the EOSPAC Interface**

- SESAME data tables are inverted at initialization and stored
- Interpolations performed using groups of common material cells
- Sorted arrays passed to EOSPAC for interpolation



Figure 2: Timing and performance data for FlecSALE runs with various integration techniques. Inversion/grouping speeds up the code by a factor of 1.5, adding sorting increases it to a factor of 1.6-1.7

# Performance Study and Optimization of FleCSALE using Tabular Equation of State

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#### **GPU Porting of EOSPAC Interpolation**

- Interpolation algorithms are single threaded but easily parallelizable
- Broadwell CPU and a Tesla P100 GPU used for performance runs



#### Machine Learning for Equation of State

- random forest (RF) regression models
- Machine learning was used to replace EOSPAC calls in FleCSALE • DLIB C++ ML library offers kernel ridge regression (KRR) and
- ML memory usage highly dependent on model



Figure 5: Absolute error of random forest model compared to EOSPAC

### **OpenMP in FleCSALE**

- OpenMP was used in outer for-loop work-sharing constructs in FleCSALE tasks
- This was tested on Intel Haswell E5-2698 v3 (2 sockets, 16 cores per socket, 2 threads per core, 64 logical cores in total) with a 200x81 mesh







Figure 4: Relative difference between the serial and CUDA implementations

Figure 6: Integration of KRR ML with FleCSALE

### **Sparse Data Optimization for FleCSI**

- MPI\_Win\_create calls was the most communication time





### **Summary and Future Work**

- FleCSALE
- expected results



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• Sparse data optimizations for FleCSI show  $\sim$ 5x speedup, but further investigation is required for MPI one-sided communication • CUDA results are promising, but still require integration with

• Initial machine learning integration was able to reproduce the



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